AMENDMENTS TO THE CLAIMS

Claims 1 – 33 (cancelled)

34. (withdrawn) A method of reading a resistive memory device comprising a plurality of stacked layers of resistive memory cells, each layer comprising an array of memory cells arranged in rows and columns, said method comprising:

accessing a selected memory cell by activating a row line coupled to a first side of said selected memory cell and turning on an access transistor which couples a second side of a plurality of memory cells in the same column of said layer, to a sense amplifier.

35. (withdrawn) A method as in claim 34, wherein said resistive memory cells are MRAM memory cells.

36. (withdrawn) A method as in claim 34 further comprising sensing a resistance value of a selected memory cell with said sense amplifier.

Claims 37 – 61 (cancelled)

62. (Currently amended) A method of reading a resistive memory device comprising a plurality of [[slices of resistive memory cells, each slice comprising an array of memory cells arranged in rows and columns]] stacked layers of resistive memory cells, each layer comprising an array of memory cells arranged in rows and columns in an X-Y plane, said plurality of stacked layers forming a plurality of slices of resistive memory cells, each slice arranged in rows and columns in Y-Z planes and having an associated access transistor, said method comprising:

applying a voltage to a read/write line associated with a selected memory cell from one of said plurality of slices of resistive memory cells;

activating an access transistor associated with said selected memory cell;

coupling selected memory cell through said selected memory cell to a sense amplifier; and

sensing a logic state of said selected memory cell.

63. (previously presented) The method as in claim 62, further comprising the step of coupling said access transistor to said selected memory cell through a sense line interconnect associated with said selected memory cell.

64. (previously presented) The method as in claim 62, further comprising the step of coupling said access transistor to said selected memory cell through a sense line associated with said selected memory cell.

65. (previously presented) The method as in claim 64, further comprising the step of coupling said access transistor to said sense line through a sense line interconnect associated with said selected memory cell.

66. (currently amended) A method of reading a resistive memory device comprising a plurality of [[slices of resistive memory cells, each slice comprising an array of memory cells arranged in rows and columns]] stacked layers of resistive memory cells, each layer comprising an array of memory cells arranged in rows and columns in an X-Y plane, said plurality of stacked layers forming a plurality of slices of resistive memory cells, each slice arranged in rows and columns in Y-Z planes and having an associated access transistor, said method comprising:

decoding an address associated with a selected memory cell in said memory device;

applying a voltage to a read/write line associated said address;

activating an access transistor associated with said address; and

sensing a logic state of said selected memory cell at said address.

67. (previously presented) The method as in claim 66, further comprising the step of determining a row address of said memory device from said address of said selected memory cell.

68. (previously presented) The method as in claim 66, further comprising the step of determining a layer address of said memory device from said address of said selected memory cell.

69. (previously presented) The method as in claim 66, further comprising the step of determining said access transistor from said address of said selected memory cell.

70. (currently amended) A method of reading a resistive memory device comprising a plurality of [[slices of resistive memory cells, each slice comprising an array of memory cells arranged in rows and columns]] stacked layers of resistive memory cells, each layer comprising an array of memory cells arranged in rows and columns in an X-Y plane, said plurality of stacked layers forming a plurality of slices of resistive memory cells, each slice arranged in rows and columns in Y-Z planes and an associated access transistor, said method comprising:

determining the X axis direction of a column decode signal associated with a selected memory cell;

determining the Y-Z plane direction of a row decode signal associated with said selected memory cell;

reading a resistance level of said selected memory cell; and

determining a logic state of said selected memory cell from said resistance level.

71. (withdrawn) The method of claim 70, further comprising comparing the resistance level to a reference level.

72. (withdrawn) The method of claim 70, wherein said reference level is a reference voltage.

73. (withdrawn) The method of claim 70, wherein said reference level is a non-addressed line of said memory device.